## *Complete Listing of the Claims*

1. (Original) An apparatus for frequency dividing a master clock signal in a system including:

a first circuit portion including a synchronous counter, the synchronous counter including at least a first group of bistable devices, each including an output port and being configured (i) to receive as an input a master clock signal and (ii) to produce an output signal at the output port in response to receiving the master clock signal; and

at least a second circuit portion including a plurality of stages, each stage including at least one bistable device from a second group of bistable devices and being coupled, at least indirectly, to one of the output ports and with the other stages to produce an output clock signal;

the apparatus comprising:

means for successively driving each of the bistable devices of the first group using the master clock signal;

means for providing selected ones of the output signals produced at the output ports of the bistable devices of the first group to inputs of respective ones of the bistable devices of the second group;

means for shifting a phase of the master clock signal to produce phase shifted versions of the master clock signal;

means for driving each of the plurality of stages with at least one of the phase shifted versions; and

means for combining outputs of the plurality of stages to produce the output clock signal;

wherein a frequency of the output clock signal is equal to a frequency of the master clock signal divided by a non-integer value.

2. (Original) An apparatus for generating a frequency divided output clock signal comprising:

means for receiving a master clock signal;

means for clocking a sequential counter having multiple outputs using the received master clock signal;

means for introducing respective outputs of the multiple outputs to respective circuit stages;

means for shifting a phase of the master clock signal to produce a plurality of phase shifted versions thereof;

means for clocking each of the respective circuit stages using at least one of the phase shifted versions of the master clock signal; and

means for combining outputs of the respective circuit stages to produce a frequency-divided output clock signal, the frequency divided output clock signal having a frequency equal to a frequency of the master clock signal divided by a non-integer value.